IN THE SPECIFICATION

Please replace the paragraph beginning at page 9, line 26, with the following rewritten paragraph:

In the recording mode, a signal to be recorded is output from a record signal processing circuit 19 to a laser diode driver (LDD) 20 under the control of the controller 18. Thereby, laser light from the ~~PUP~~ PUH 12 is modulated and information is recorded onto recording tracks of the optical disc 11.

Please replace the paragraph beginning at page 13, line 23, with the following rewritten paragraph:

The wobble signal having noise removed is applied to a phase detector 32 and at the same time to a phase-locked loop (PLL) ~~circuit~~ 33 to produce a carrier signal. In the phase-locked loop circuit 33, the phase locking function is performed to produce a carrier signal that is locked to the wobble signal, which is shown in FIG. 12C. In the phase detector 32, phase detection is performed on the basis of the wobble signal and the carrier locked to it. A typical method of phase detection is to discriminate between phases through multiplication of a modulated signal and a carrier signal.

Please replace the paragraph beginning at page 24, line 12, with the following rewritten paragraph:

FIG. 27 illustrates an address detection method using an integrator 71 and its associated error rate measurement method. In FIG. 27, each of the corresponding components to those in the demodulation circuit shown in FIG. 11 is denoted by a like reference numeral. The output of the phase detector 32, after being subjected to low-pass filtering and slicing, is input to the symbol clock generator [[71]] 36 to generate the symbol clock. The phase detector output is also applied to the integrator 71 that can be reset. The symbol clock is also

applied to the integrator 71. The integrator 71 integrates and outputs the input phase detector output waveform at regular intervals separated by the symbol clock period. This operation is illustrated in FIG. 28. On the output side of the integrator 71 is placed a register that holds an integration value at the time when each symbol clock pulse is input. The value in the register is updated with each symbol clock pulse. The calculated value at the time of integration processing is reset upon entry of the symbol clock. The waveform thus obtained is input to the address decoder 72 together with the symbol clock, whereby addresses are decoded. The address data obtained by the address decoder 72 is applied to the succeeding address error rate calculator 73, which performs synchronization processing on the address map from the previously prepared ~~memory~~ address map 74 and the input address data to calculate the address error rate. To ensure the reliability at the time when this detection system is used, it is desirable that the address error rate be less than 1E-3, as in the foregoing case.

Please replace the paragraph beginning at page 24, line 12, with the following rewritten paragraph: